A MONOLITHIC GaAs 3-BIT PHASE QUANTIZATION SAMPLER

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ABSTRACT

This paper describes the analysis, design, and development of a high-speed A/D and D/A converter using phase-quantization sampling. A monolithic GaAs A/D and D/A converter has been demonstrated within a RF signal acquisition system. Performance data on the monolithic IC reveals that the 3-bit quantization system exhibits signal reconstruction with harmonic suppression exceeding -25 dB across an IF bandwidth of greater than 900 MHz.

INTRODUCTION

RF signal acquisition subsystems, such as digital radio frequency memory (DRFM) [1-3], are developing into an essential part of both electronic countermeasure (ECM) systems and the automatic test equipment (ATE) with which these ECM systems must be functionally tested. The basic function of a DRFM is to sample an incident RF signal, store the digitized sample of the waveform for a programmed period of time, and then reconstitute the signal at the input intermediate frequency (IF) upon command from a controller. The sampled signal data stream(s) can be digitally manipulated to regenerate the incident waveform in either a delayed or continuous form, or, as is the case within an ATE application, software and/or hardware mathematical transforms can be used on the stored data to perform complex signal analysis and measurement.

The frequency limitations of operation depend primarily on the RF downconversion prior to signal sampling and storage, and the RF upconversion system used to regenerate the RF input. The function of a DRFM within a typical ECM system is shown in Figure 1.

The key hardware elements of these types of systems are the A/D, D/A, shift registers for data multiplexion, and RAM for data storage and retrieval.

The 8-bit shift registers to perform the serial-to-parallel and parallel-to-serial data stream conversions have been shown working at 1.14-GHz clock rate using GaAs technology [2]. By using Si CMOS, the shift registers and RAMs integrating on the same chip have been shown working at 0.5 GHz for a 1-bit system [3]. GaAs A/D converters have been shown with steady advancements every year [4-10].

Honeywell is involved in developing and applying these elements within ECM subsystems and their associated ATE. An element of this development includes the design, fabrication, and test of GaAs depletion-mode and enhancement-mode circuits [1, 11-12].

In this paper we describe a 3-bit sampler for use in a DRFM system, including the front-end analog-to-digital converter (ADC) and the back-end digital-to-analog converter (DAC), without the shift registers and memory elements.

WHY PHASE QUANTIZATION?

The phase-sampling technique is used to implement this IC. Figure 2 shows the difference between amplitude and phase quantization.

The phase approach has some key advantages over the conventional amplitude digitization technique for a 3-bit system. The near-harmonic suppression is improved; the worst-case harmonic for the amplitude technique is the third harmonic while for the phase approach it is the seventh harmonic. The phase digitization technique is theoretically independent of signal amplitude, thus eliminating dynamic range problems typically associated with amplitude systems.

COMPARATOR AND SUMMER REQUIREMENTS

One must first quantify the effects of comparator and latch parameters such as offset, bandwidth, impedance, common mode rejection, and other critical circuit parameters on phase error. Phase error sensitivity of each of these critical parameters must also be investigated, as well as the effects of sampling error upon the harmonic spectra of the digitizer waveform. For example, given an input frequency of 250 MHz (4-ns period), the phase shift between the comparators in a 3-bit phase quantization sampler would be 45 deg. If an error of 1 part in 10 was allowed, a time accuracy of 50 psec and a phase accuracy of 4.5 deg would be required. In the case of a current summing amplifier used as a D/A converter, such parameters as level weighting, bandwidth, output drive, linearity, switching speed, etc., become critical factors relative to frequency accuracy and harmonic performance.

System tradeoffs must be performed to weigh quantization level versus complexity within the specified application in order to determine the

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most simple, realizable, and cost-effective design approach. The hardware interface to conventional ECL and TTL/CMOS circuits must also be considered as part of the monolithic IC design approach.

3-BIT PHASE QUANTIZATION SAMPLER

A monolithic GaAs 3-bit phase sampling system (ADC and DAC) has been implemented in an RF signal acquisition system. Figure 3 shows the block diagram of the 3-bit GaAs sampler IC, including the RF section, which allows the IC to digitize signals at RFs up to 6 GHz. The significance of the work is to demonstrate the feasibility of integrating GaAs analog and digital ICs together with microwave components.

The sampler IC is a custom monolithic, multibit phase digitizer and recombiner consisting of an input signal conditioning network, a bank of four dual-stage comparators [4], and two active summer circuits [5]. Figure 4 shows the circuit schematic of the 3-bit sampler. Quadrature RF input signals are conditioned and then phase-angle quantized by the comparators. Each of the four dual-stage comparators samples the input signal at 45-deg intervals with respect to each other (A/D function). The active summer circuits receive the binary information generated from the four comparators and combines it to reproduce quadrature analog outputs at the identical frequency of the input signal (D/A function). The digital data input to the summing networks is amplitude weighted to optimize the spurious rejection of the output waveforms.

This 3-bit sampler has been designed, fabricated, and tested using GaAs nonself-aligned depletion-mode MESFETs with a threshold voltage of -1.3V [1]. Figure 5 is a photograph of the fabricated IC. The dimensions of this IC are approximately 40 x 60 mils.

We performed circuit simulation of the 3-bit phase sampler to verify the system concept at the circuit level. Figure 6 shows reconstructed signals (I^- and I^+) at 100 Hz, 100 MHz, and 500 MHz using the modified SPICE JFET model for GaAs MESFET [1]. Figure 6 indicates the expected performance of the 3-bit phase sampler, which will be operational at frequencies approaching 500 MHz. Table 1 summarizes the simulated performance of the 3-bit phase quantization sampler. The output signal amplitude (I and Q) is down 3 dB at approximately 600 MHz. A comparison of the predicted frequency performance versus measured data at 400 MHz shows a correlation to within 30%.

The chip has been tested at the wafer level using a high-frequency probe card, with the test set up as shown in Figure 3.

Measured data shows that a 900-MHz input signal was digitized and recombined in quadrature with an output amplitude of 70 mV_{pp} into a 50Ω load impedance. The 3-dB output bandwidth was 400 MHz, and the nominal low-frequency output voltage was 420 mV_{pp}. Spectrum analysis shows harmonic suppression greater than -25 dB across the band of 10 to 900 MHz. Figure 7 shows the output waveform at 900 MHz and its frequency spectrum, and Figure 8 shows the reconstructed signal at a frequency of 200 MHz.

These test results have provided the data required for an improved GaAs design for DRFM applications requiring larger bandwidths and increased resolution as described in [1,11-12].

COMPARATOR AND SUMMER

The depletion-mode comparator used in the 3-bit sampler has been simulated and tested for both DC and AC data [4].

Figure 9 shows the simulated output response of the comparator's pre-amplifier relative to input overdrives. The pre-amp does not respond until it is overdriven by at least 20 mV. The response time is 300 ps with 400-mV input overdrive.

The test structure of the dual-stage comparator has a source follower for driving 50Ω capacitive loads. Figure 10 shows clock and output waveforms of the dual-stage comparator under varying test conditions. The low-frequency performance shown in Figure 10 reflects a 3-bit linearity. The typical resolution voltage is 200 mV with a common-mode voltage larger than 1.5V.

Figure 10c shows input and output waveform rise and fall times, which translate into a conversion time of 750 ps.

The summer circuit used in the 3-bit DRFM sampler is a monolithic 4-bit DAC as shown in Figure 4 [5]. Figure 6a shows the simulated results of the output response at low frequency with amplitude-weighted quantization levels.

The summer has been tested and has shown a 5-bit linearity with an amplitude weighting as shown in Figure 11. A typical resolution voltage is 50 mV with a common-mode voltage larger than 1.5V. The measured output rise and fall times are 500 ps into a 50Ω 3-pF load. This suggests that the bandwidth of the summer is about 700 MHz ($BW = 0.35/t_r$).

The summer operates with a clock frequency of up to 200 MHz, demonstrated in a DRFM brassboard. The speed limitation is primarily due to the clock speed of the Si ECL components.

ACKNOWLEDGMENTS

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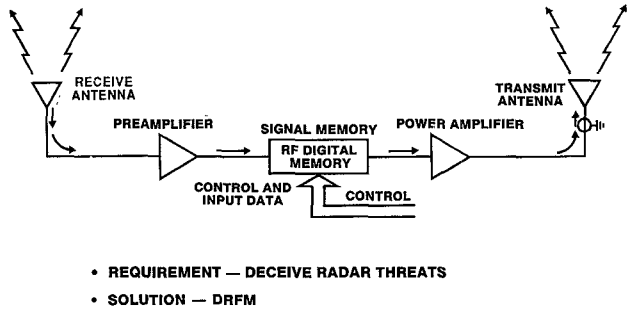
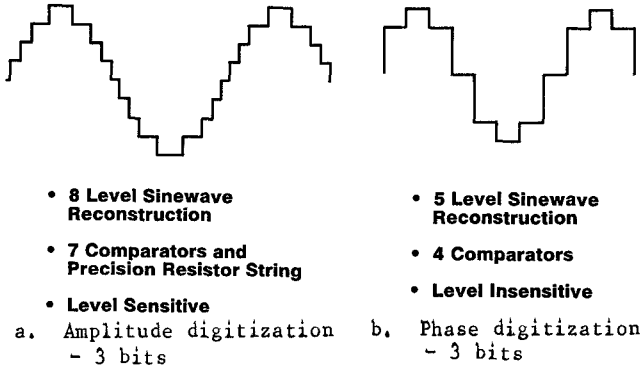


Figure 1. DRFM as Part of an ECM System



a. Amplitude digitization - 3 bits

b. Phase digitization - 3 bits

Figure 2. Comparison of Phase and Amplitude Digitization

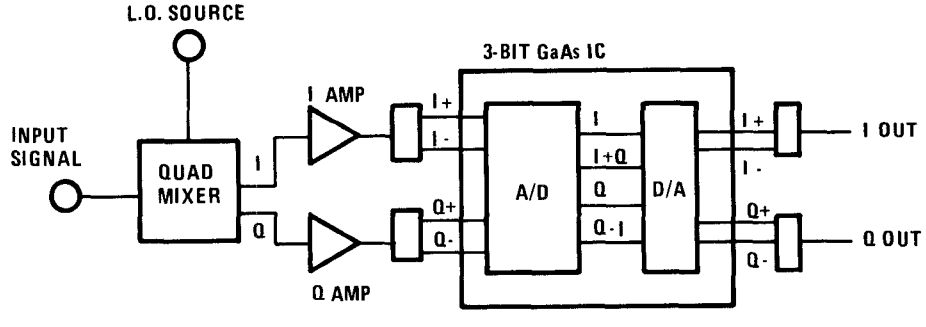


Figure 3. Text Set-Up for the 3-Bit A/D and D/A Sampler

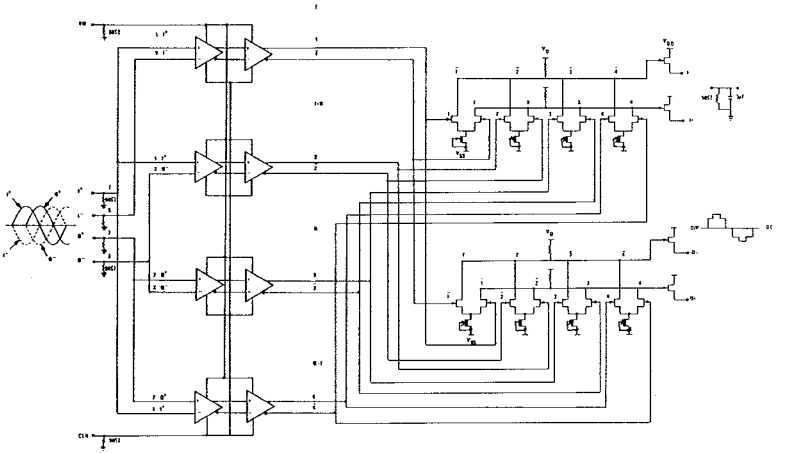


Figure 4. Circuit Schematic of the GaAs 3-Bit Sampler

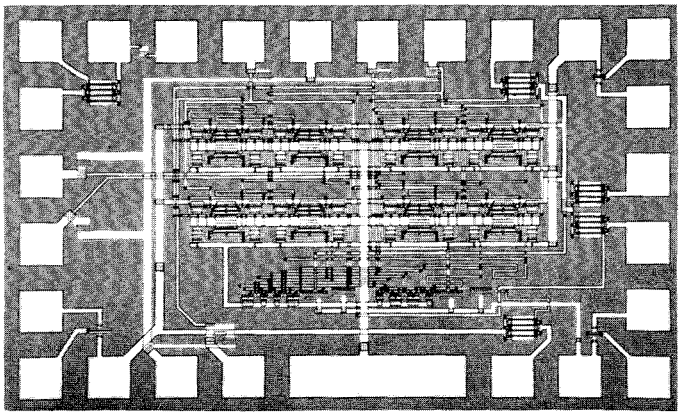
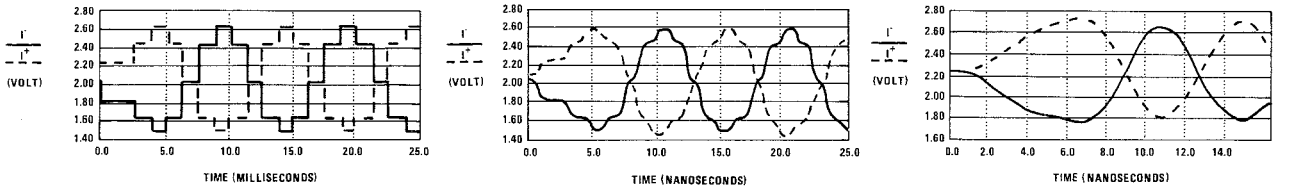
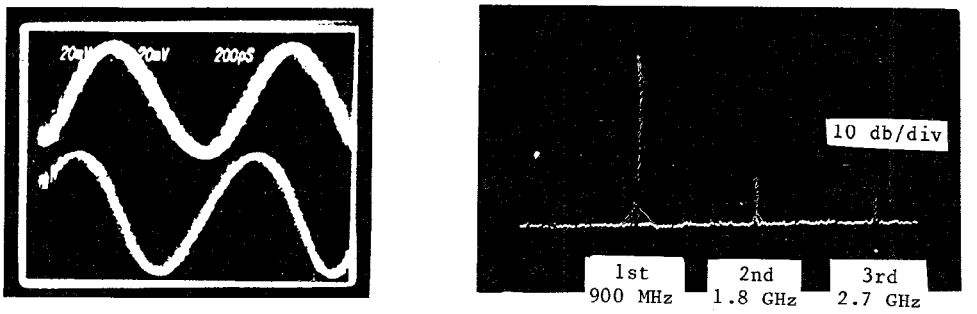


Figure 5. Photograph of the GaAs 3-Bit Sampler IC



a. 100 Hz b. 100 MHz c. 500 MHz

Figure 6. Simulated Outputs of the Reconstructed Signals (I^+ and I^-) versus Input Frequencies



a. Output at F_{IN} = 900 MHz b. Frequency spectrum of output

Figure 7. High-Speed Waveforms of the 3-Bit Sampler

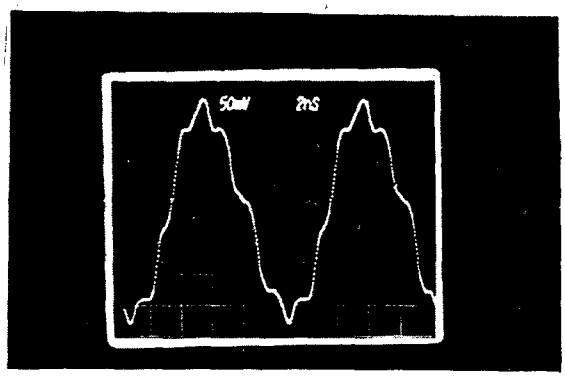


Figure 8. Quantized 200-MHz Output Obtained from the GaAs 3-Bit Sampler IC

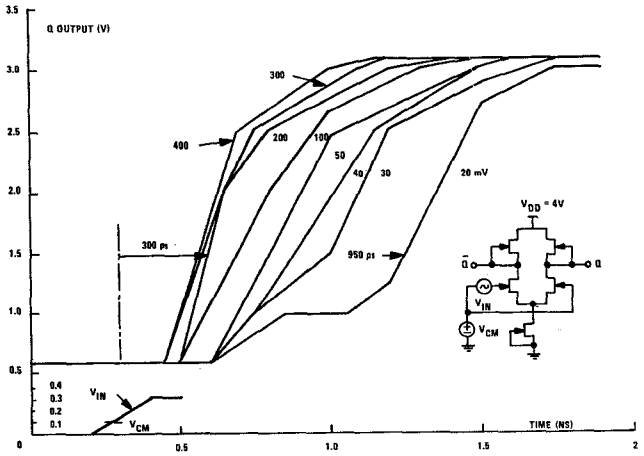
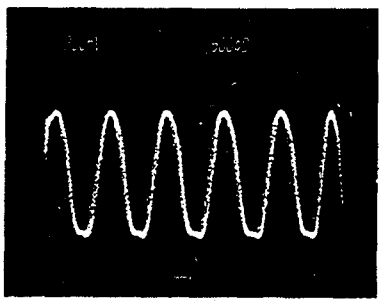
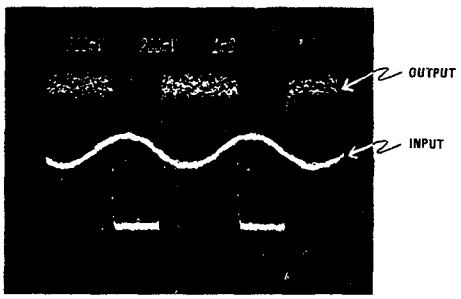


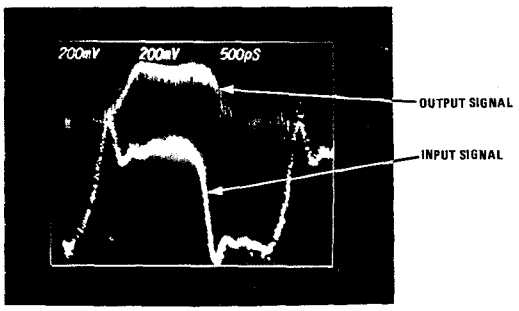
Figure 9. Output Response of Comparator's Pre-Amplifier Relative to Input Overdrives



a. 1-GHz clock



b. Input and output signals at low frequency



c. Input and output signals at high frequency

Figure 10. Waveforms of Comparators

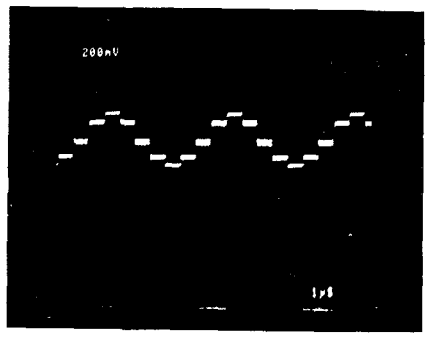


Figure 11. Output of 3-Bit Phase Quantization Summer (4-bit D/A converter)

TABLE 1. SIMULATED PERFORMANCE OF 3-BIT DRFM SAMPLER

Frequency of Input Data	Output Amplitude in Volts		Output in dB* After Output Buffer Source Follower
	Before Source Follower	After Source Follower	
100 Hz	1.6	1.15	1.21
100 MHz	1.5	1.10	0.83
500 MHz	1.2	0.9	−0.92 −3dB at 600 MHz
1 GHz	0.3	0.1	−20

*$dB = 20 \log \frac{V_o}{V_i}$, $V_i = 1V_{pp}$